

PRIOR ART

FIG. 1

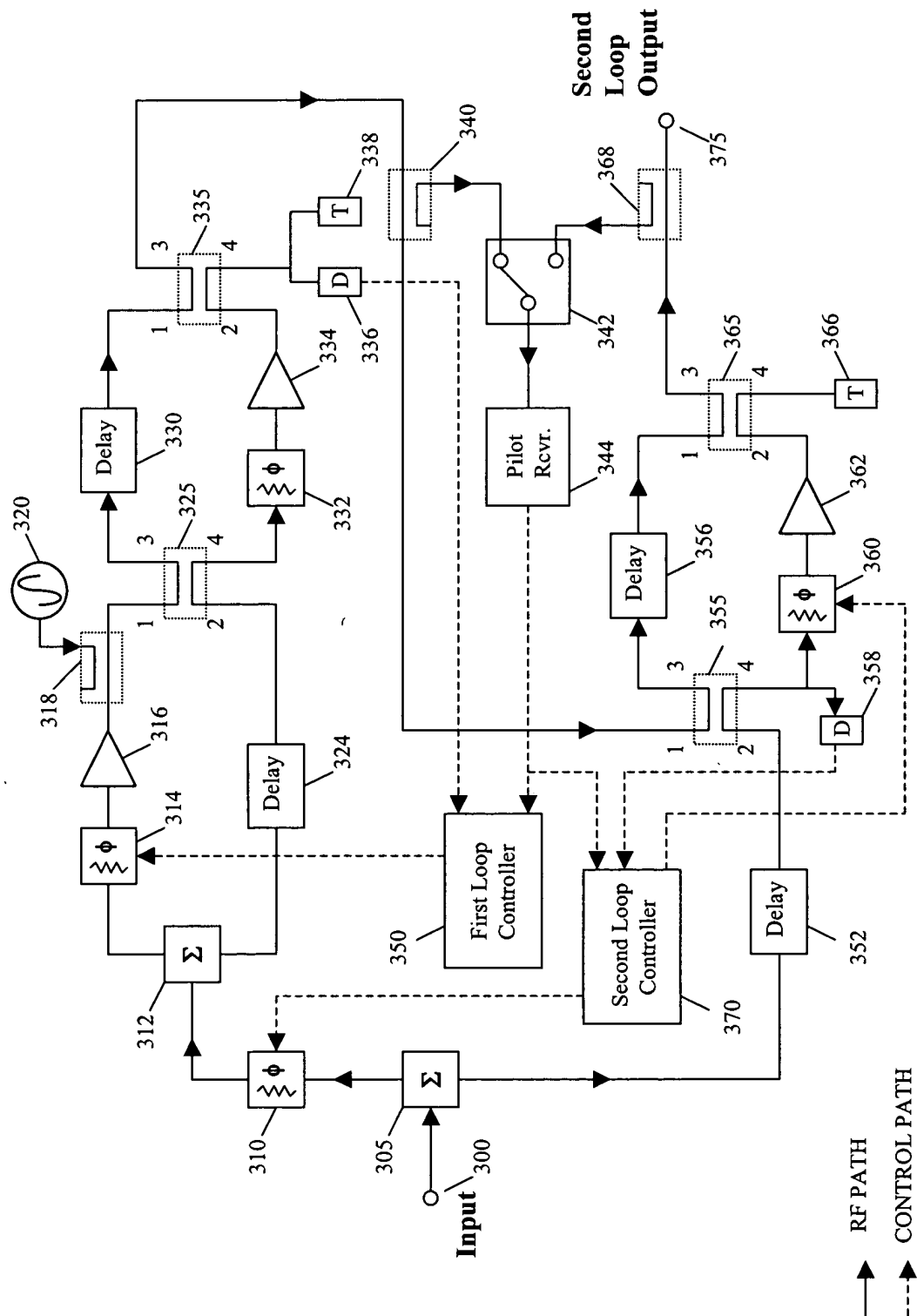
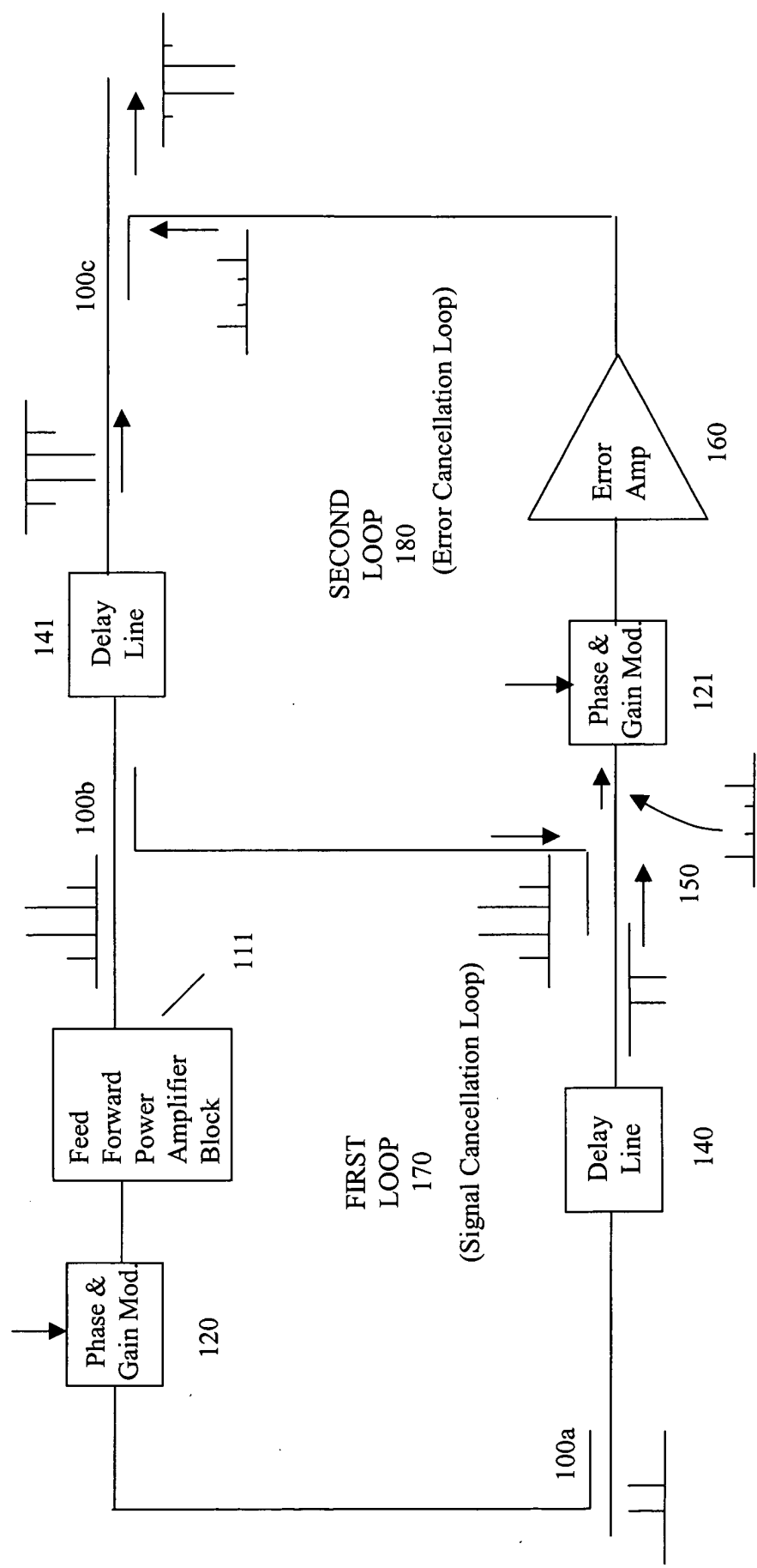


FIG. 2

PRIOR ART

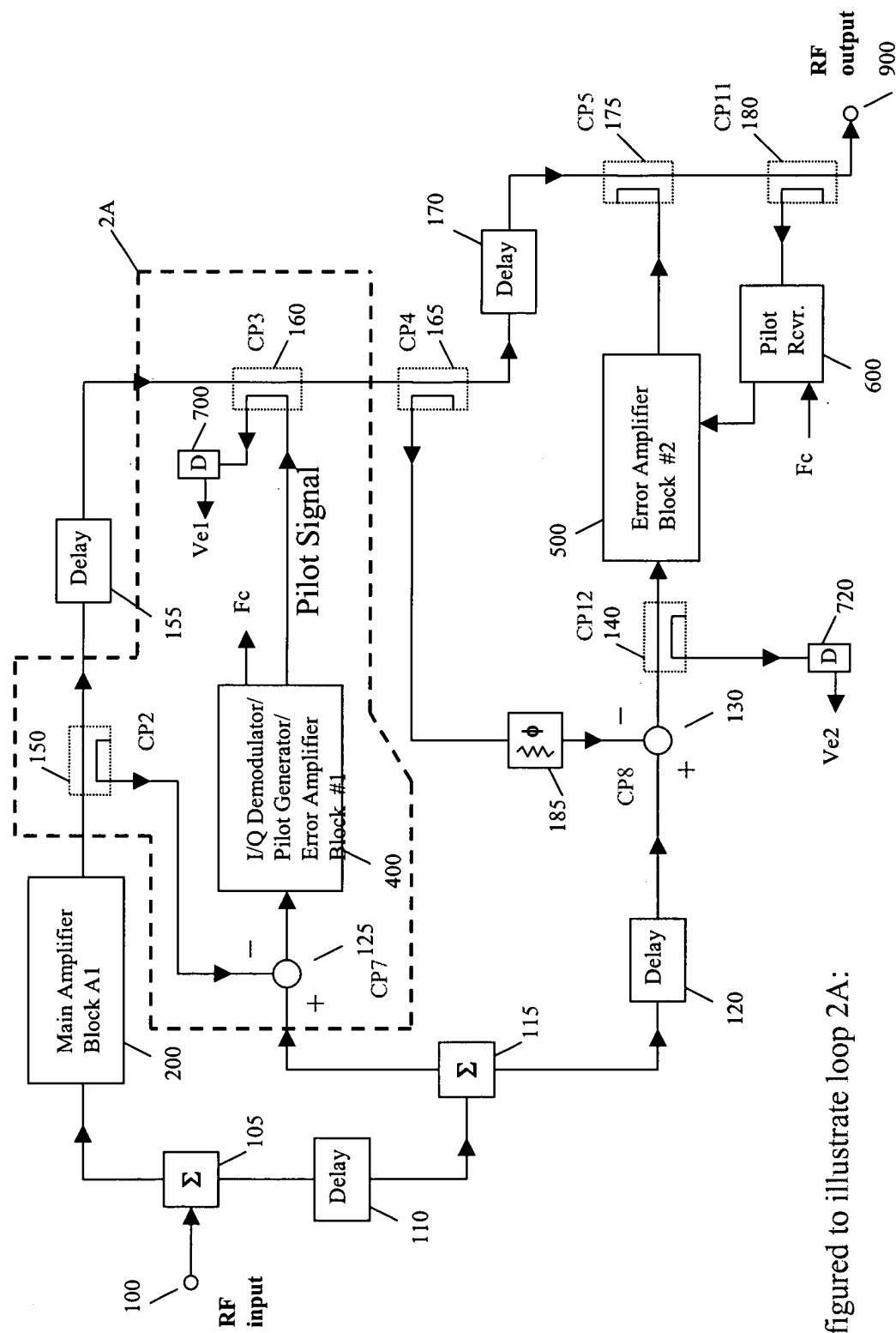


PRIOR ART

FIG. 3



FIG. 4



configured to illustrate loop 2A:

FIG. 5





FIG. 7

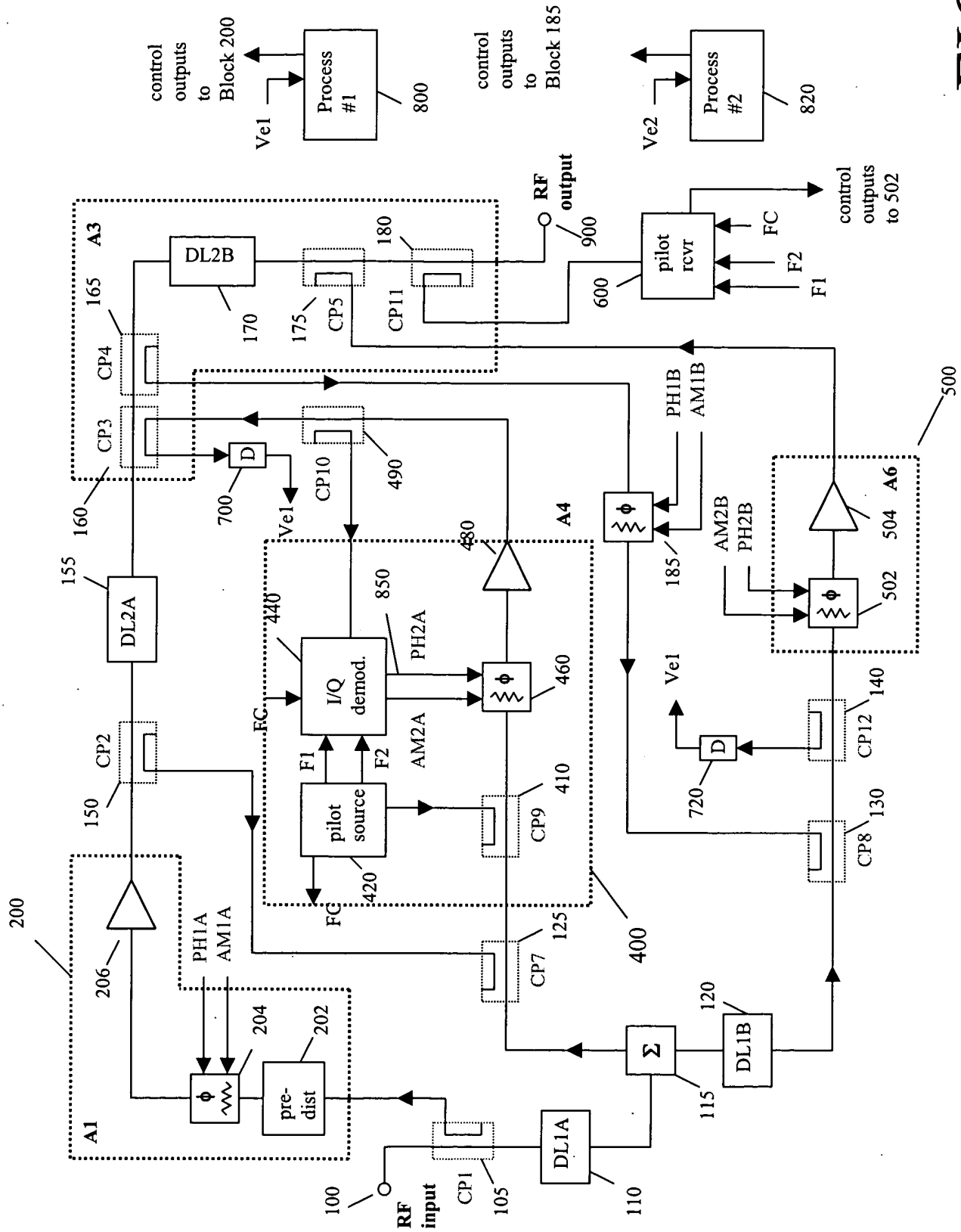


FIG. 8

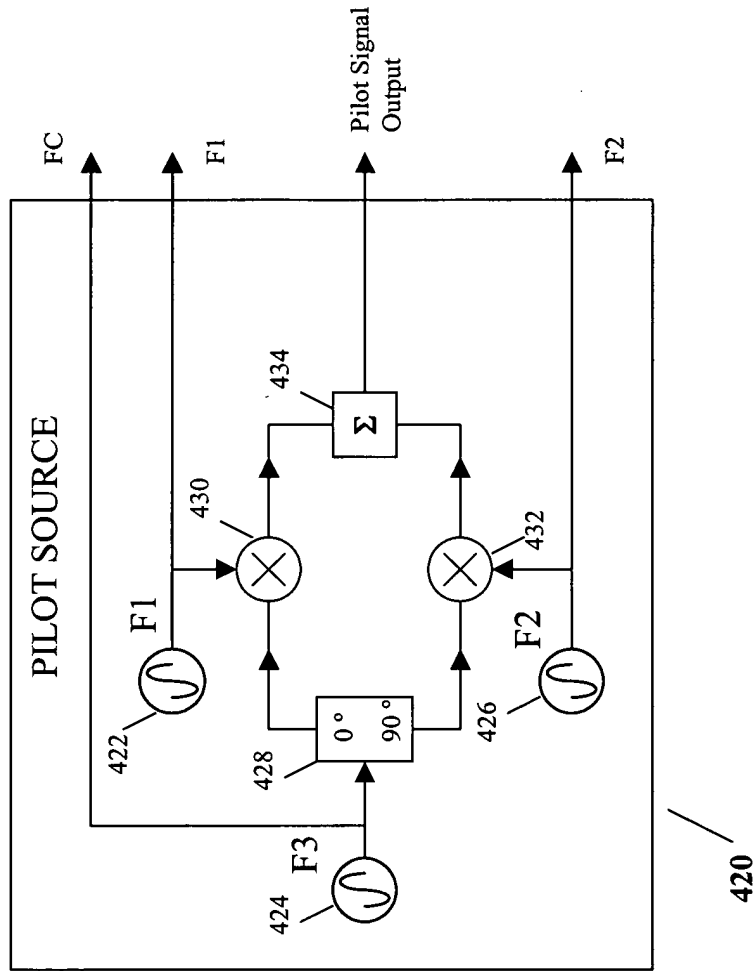


FIG. 9

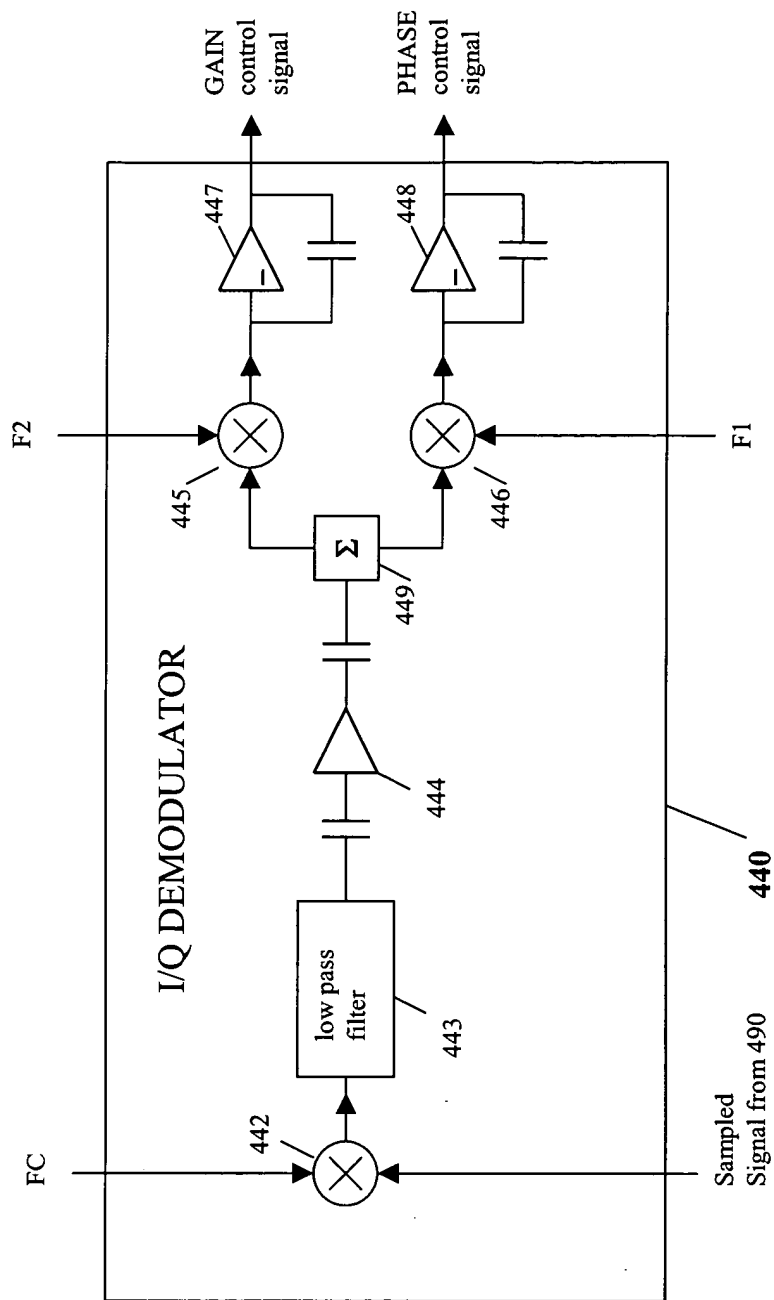


FIG. 10

[illegible]

FIG. 11

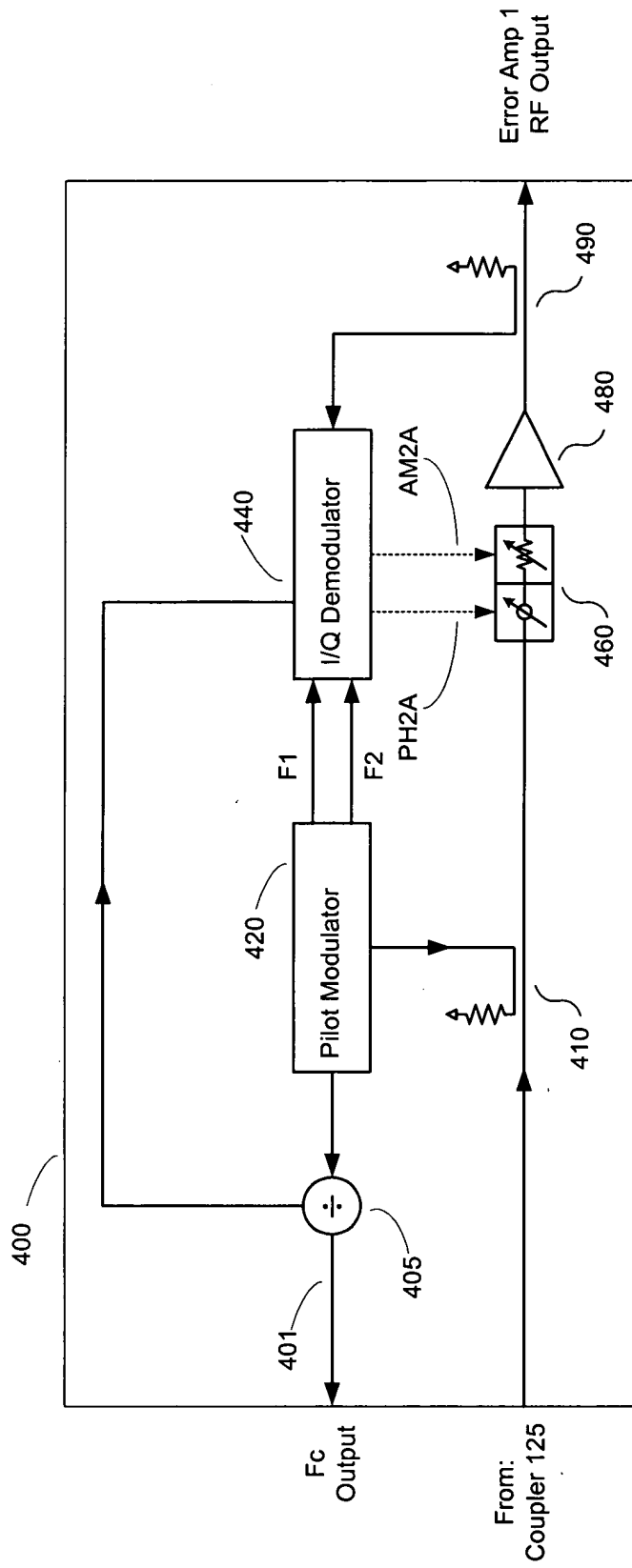
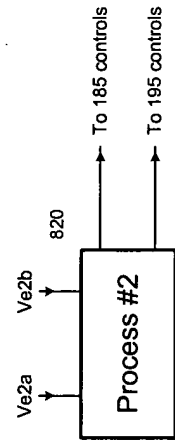


FIG. 12



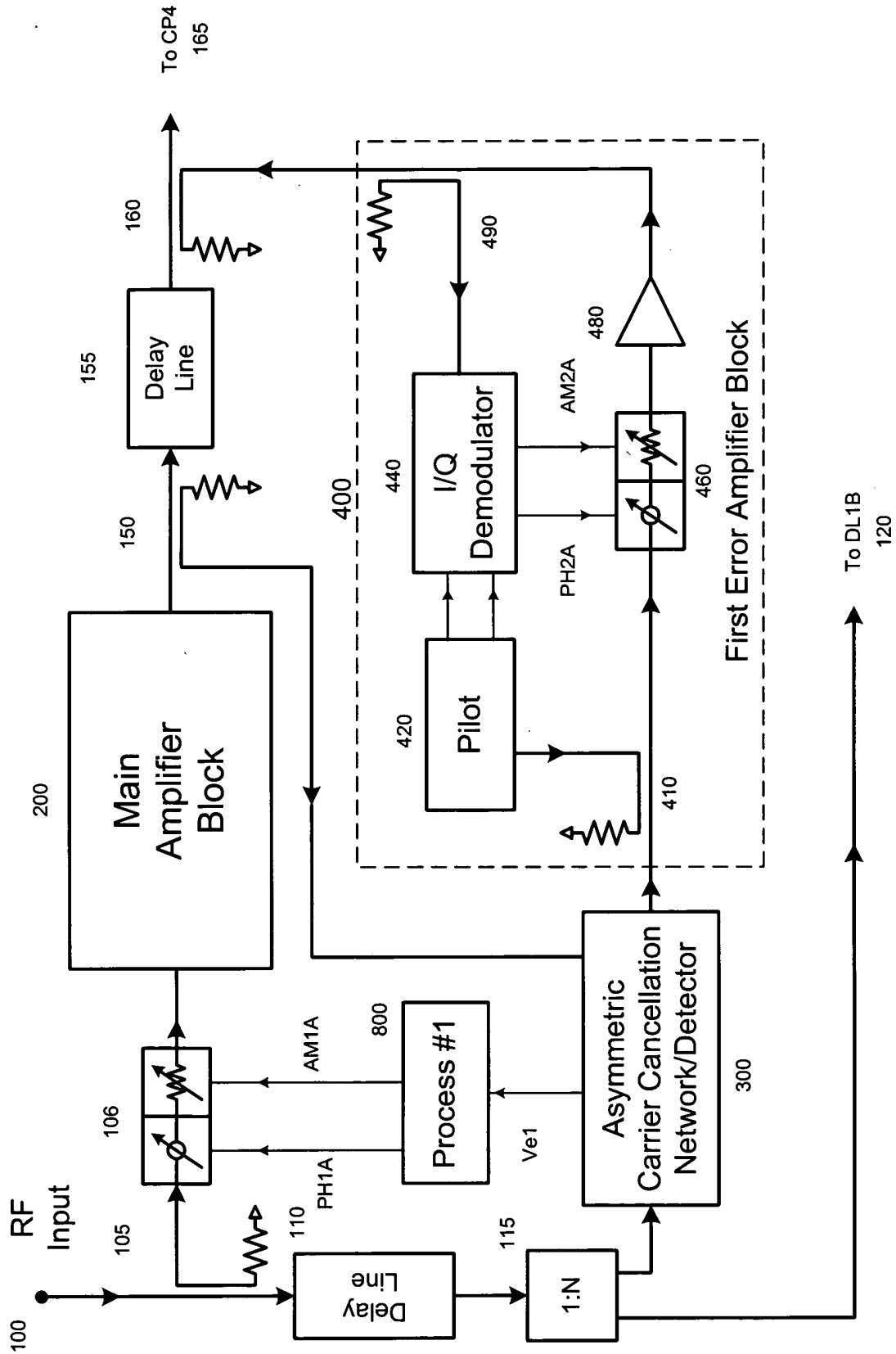
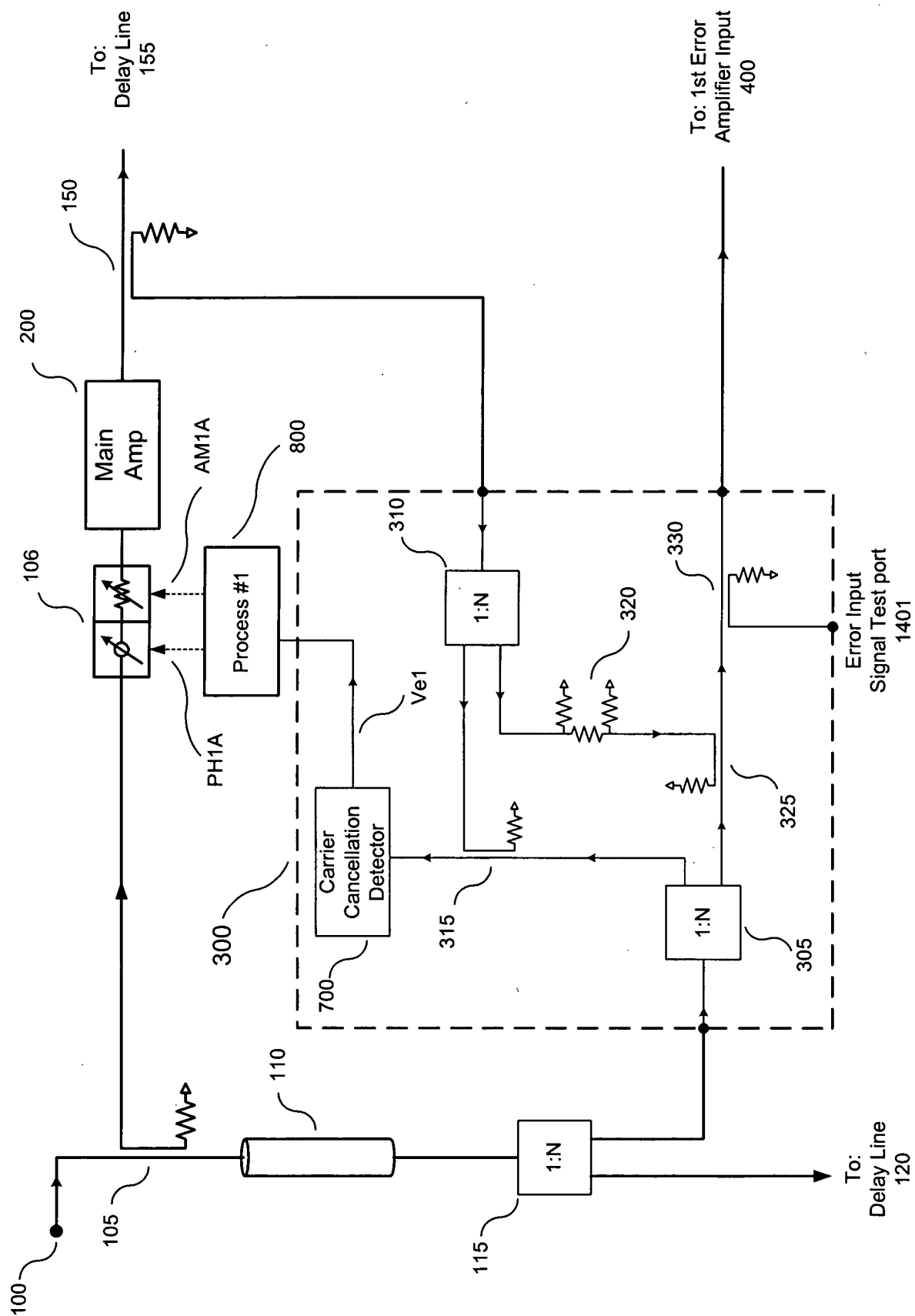


FIG. 13B



1st Error Amplifier Stabilization

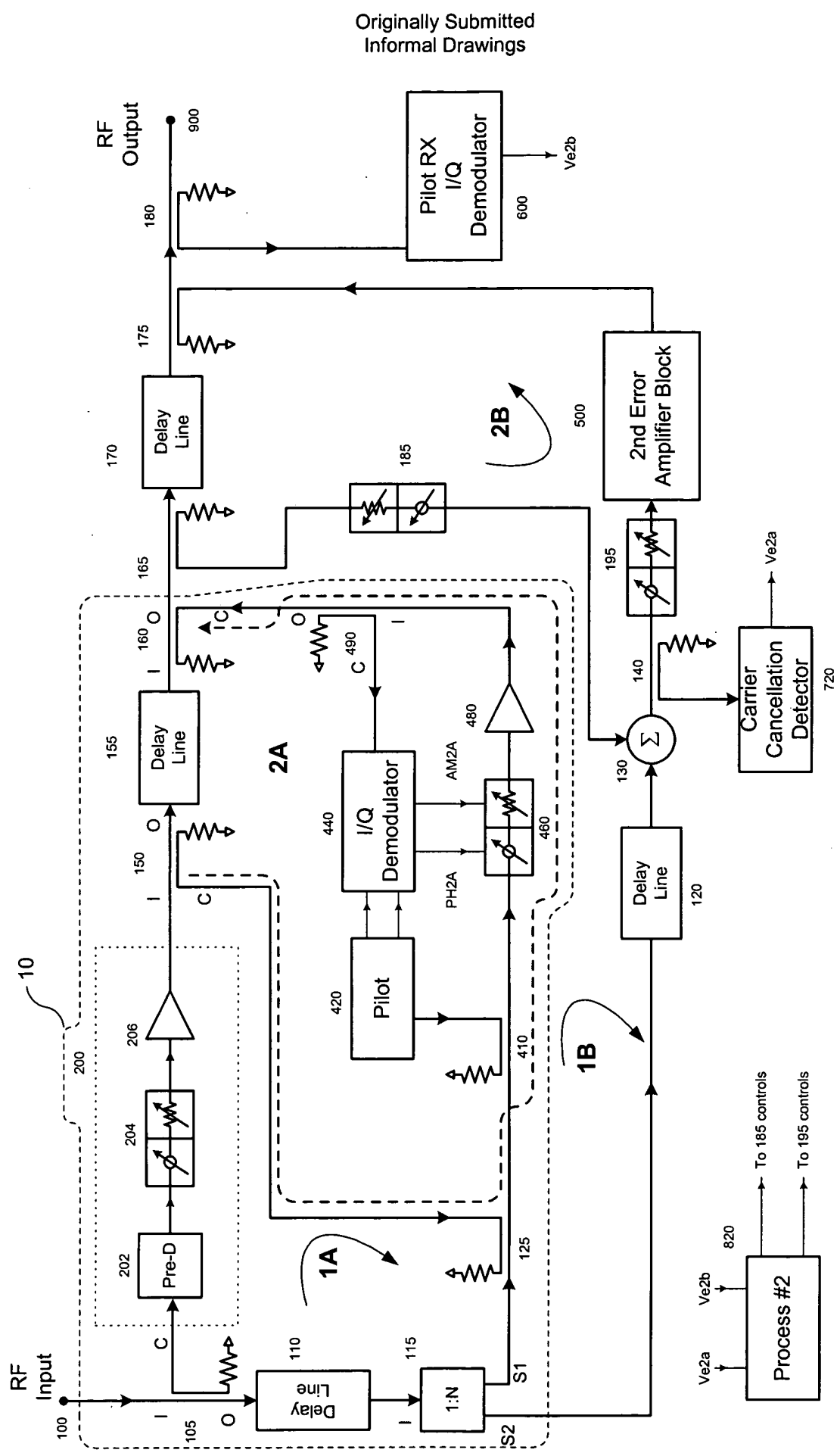
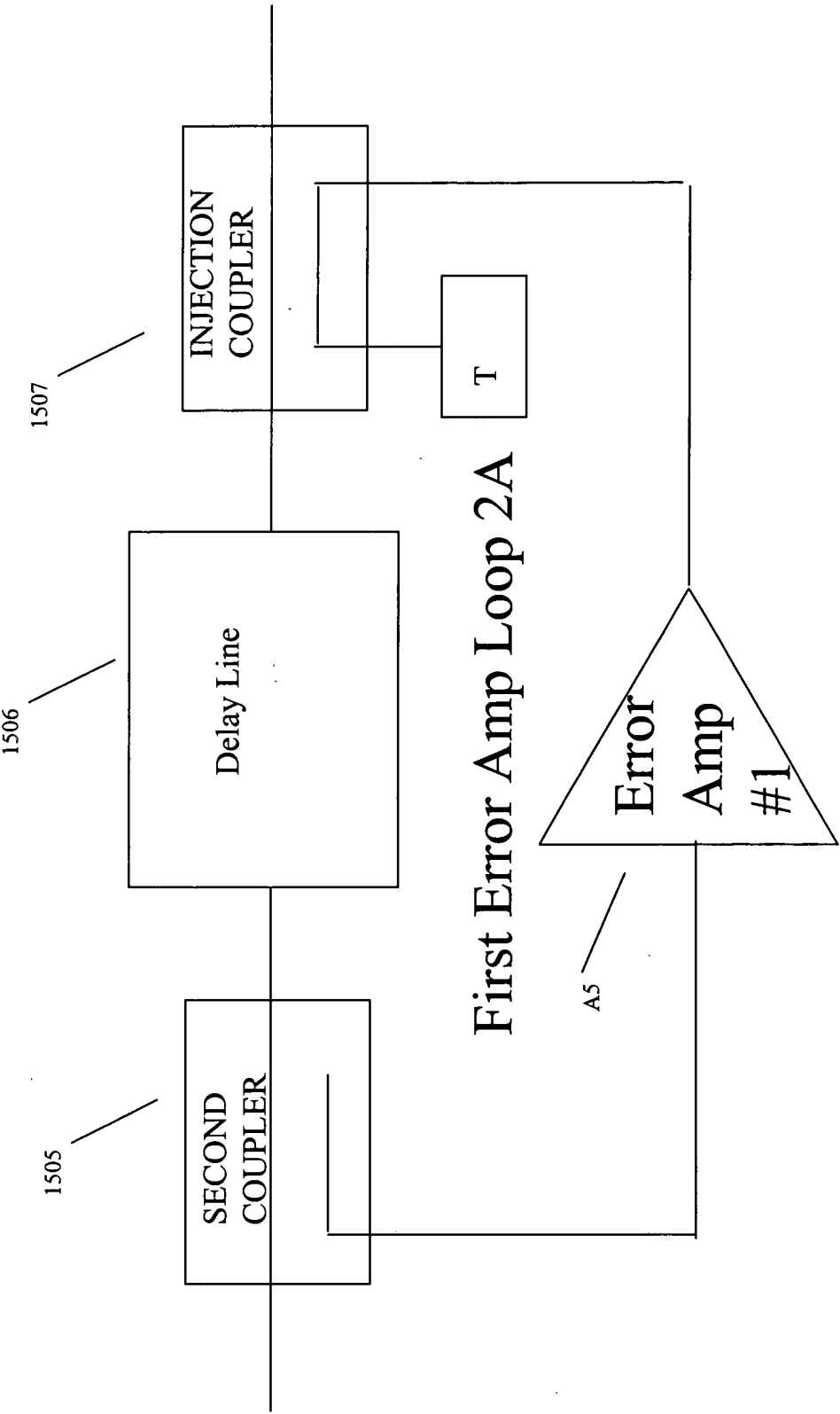


FIG. 15

Error Amplifier Stabilization



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Informal Drawings

FIG. 16

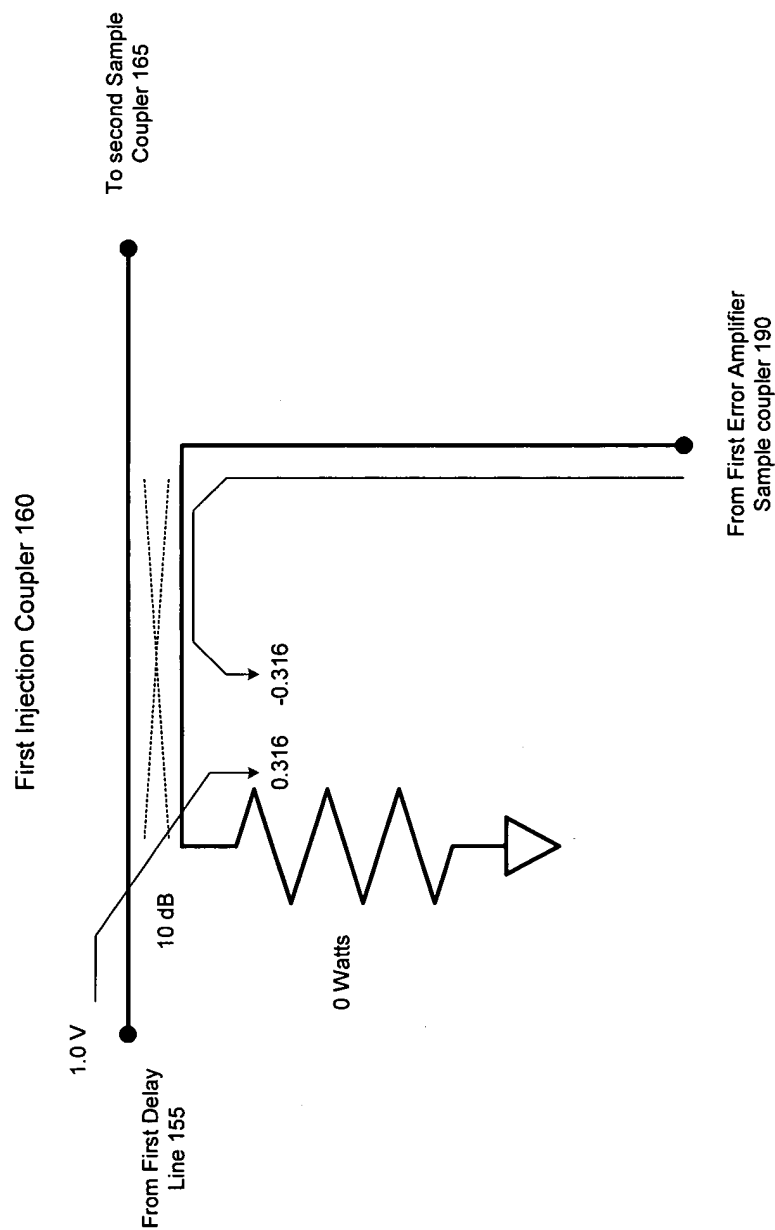


FIG. 17

Carrier Re-Injection

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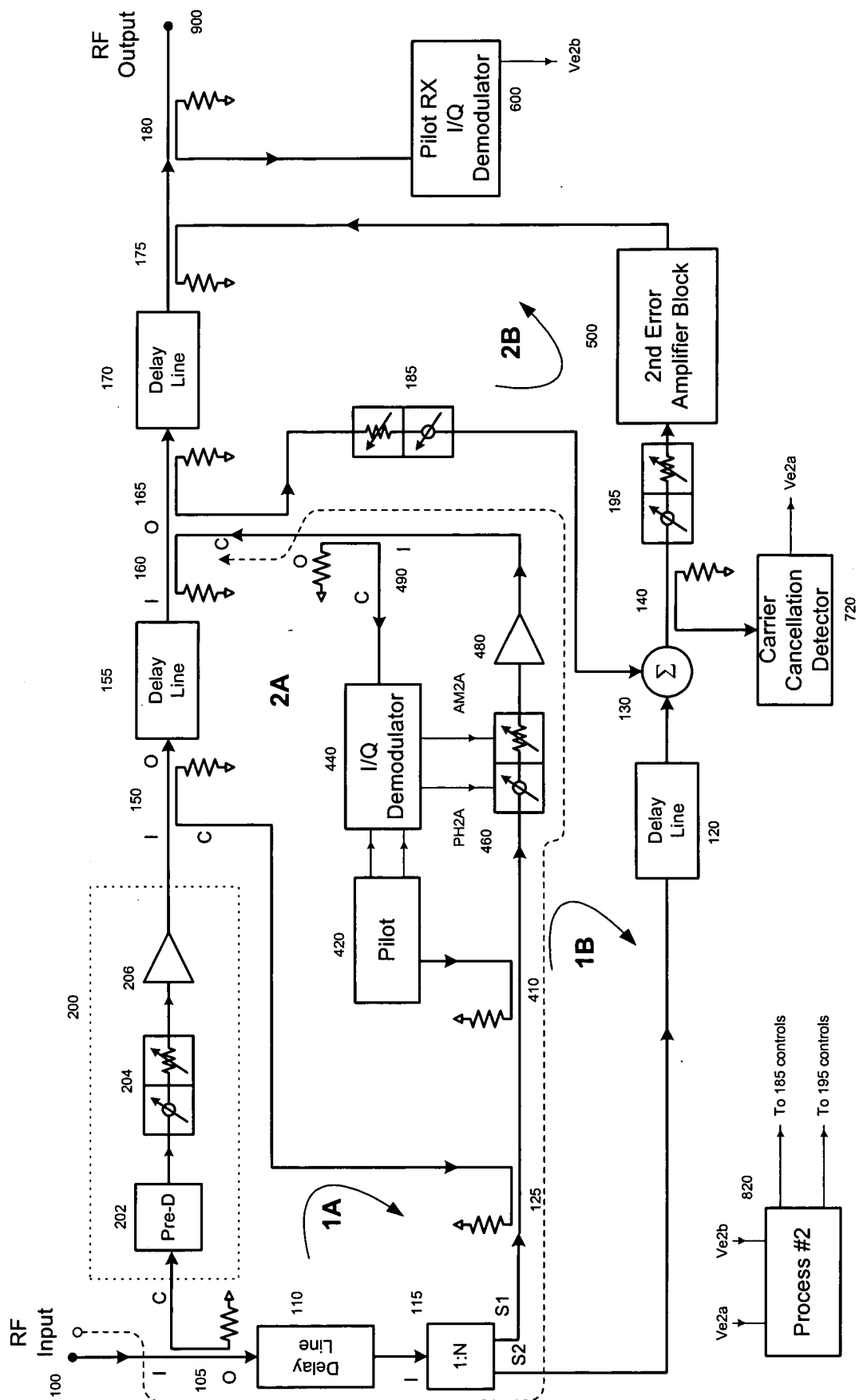


FIG. 18

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FIG. 19